;\* $Id: //depot/software/FC220/include/TE5\_CSOC.inc#3 $

;\*

;\* Triscend E5 CSoC device register definition file

;\*

;\* Copyright (c) 2000, 2001 Triscend Corporation. All rights reserved.

;\* The following macro definition is needed if you include this

;\* file directly, instead of the FastChip project header file

;\* Both FastChip project header and source file define their own

;\* macros, and set the USE\_PROJECT\_FILE\_MACRO flag to skip the

;\* following macro definitions.

$IF (USE\_PROJECT\_FILE\_MACRO)

$ELSE ;\* USE\_PROJECT\_FILE\_MACRO

;\*======== Required macro definitions ========

CHAR\_XDATA MACRO SYMNAME,SYMLOC

SYMNAME EQU SYMLOC

ENDM

CHAR\_ARRAY\_XDATA MACRO SYMNAME,SYMLOC,SIZE

SYMNAME EQU SYMLOC

ENDM

$ENDIF ;\* USE\_PROJECT\_FILE\_MACRO

;\* Assume that $NOMOD51 is placed in the top level A51 file(s)

;\* in order to prevent A51 assembler from implicitly defining

;\* symbols for the default 8051 special function registers.

;\* Alternatively, add the NOMOD51 to the assembler control string.

;\* Consult Keil documentation if needed.

;

;\*======== E5 byte addressable SFR registers ========

CSEG

; -- reserved (P0) --

SP DATA 081H

DPL DATA 082H

DPH DATA 083H

DPL1 DATA 084H

DPH1 DATA 085H

DPS DATA 086H

PCON DATA 087H

TCON DATA 088H

TMOD DATA 089H

TL0 DATA 08aH

TL1 DATA 08bH

TH0 DATA 08cH

TH1 DATA 08dH

CKCON DATA 08eH

; -- reserved (P1) --

SCON DATA 098H

SBUF DATA 099H

; -- reserved (P2) --

IE DATA 0a8H

SADDR DATA 0a9H

; -- reserved (P3) --

IP DATA 0b8H

SADEN DATA 0b9H

TA DATA 0c7H

T2CON DATA 0c8H

T2MOD DATA 0c9H

RCAP2L DATA 0caH

RCAP2H DATA 0cbH

TL2 DATA 0ccH

TH2 DATA 0cdH

PSW DATA 0d0H

WDCON DATA 0d8H

ACC DATA 0e0H

EIE DATA 0e8H

B DATA 0f0H

EIP DATA 0f8H

;\*======== E5 bit addressable SFR registers ========

;\*---------------------------- TCON

TF1 BIT 08fH

TR1 BIT 08eH

TF0 BIT 08dH

TR0 BIT 08cH

IE1 BIT 08bH

IT1 BIT 08aH

IE0 BIT 089H

IT0 BIT 088H

;\*---------------------------- SCON

SM0 BIT 09fH

SM1 BIT 09eH

SM2 BIT 09dH

REN BIT 09cH

TB8 BIT 09bH

RB8 BIT 09aH

TI BIT 099H

RI BIT 098H

;\*---------------------------- IE

EA BIT 0afH

; -- reserved --

ET2 BIT 0adH

ES BIT 0acH

ET1 BIT 0abH

EX1 BIT 0aaH

ET0 BIT 0a9H

EX0 BIT 0a8H

;\*---------------------------- IP

; -- reserved --

; -- reserved --

PT2 BIT 0bdH

PS BIT 0bcH

PT1 BIT 0bbH

PX1 BIT 0baH

PT0 BIT 0b9H

PX0 BIT 0b8H

;\*---------------------------- T2CON

TF2 BIT 0cfH

EXF2 BIT 0ceH

RCLK BIT 0cdH

TCLK BIT 0ccH

EXEN2 BIT 0cbH

TR2 BIT 0caH

C\_T2 BIT 0c9H

CP\_RL2 BIT 0c8H

;\*---------------------------- PSW

CY BIT 0d7H

AC BIT 0d6H

F0 BIT 0d5H

RS1 BIT 0d4H

RS0 BIT 0d3H

OV BIT 0d2H

P BIT 0d0H

;\*---------------------------- WDCON

POR BIT 0deH

EHPI BIT 0ddH

HPI BIT 0dcH

WDIF BIT 0dbH

WTRF BIT 0daH

EWT BIT 0d9H

RWT BIT 0d8H

;\*---------------------------- EIE

; -- reserved --

; -- reserved --

; -- reserved --

EWDI BIT 0ecH

; -- reserved --

; -- reserved --

; -- reserved --

; -- reserved --

;\*---------------------------- EIP

; -- reserved --

; -- reserved --

; -- reserved --

PWDI BIT 0fcH

; -- reserved --

; -- reserved --

; -- reserved --

; -- reserved --

;\*========= Visible CRU Registers ===

E5CRU\_VISIBLE\_BASE\_ADDR EQU 0f000H

XSEG

CHAR\_XDATA CMAP0\_TAR, 0ff00H

CHAR\_XDATA CMAP0\_ALT, 0ff01H

CHAR\_XDATA CMAP1\_TAR\_0, 0ff02H

CHAR\_XDATA CMAP1\_TAR\_1, 0ff03H

CHAR\_XDATA CMAP1\_TAR\_2, 0ff04H

CHAR\_XDATA CMAP1\_SRC, 0ff05H

CHAR\_XDATA CMAP1\_CTL, 0ff06H

CHAR\_XDATA CMAP1\_ALT, 0ff07H

CHAR\_XDATA CMAP2\_TAR\_0, 0ff08H

CHAR\_XDATA CMAP2\_TAR\_1, 0ff09H

CHAR\_XDATA CMAP2\_TAR\_2, 0ff0aH

CHAR\_XDATA CMAP2\_SRC, 0ff0bH

CHAR\_XDATA CMAP2\_CTL, 0ff0cH

CHAR\_XDATA CMAP2\_ALT, 0ff0dH

CHAR\_XDATA DMAP0\_TAR, 0ff0eH

CHAR\_XDATA DMAP1\_TAR\_0, 0ff0fH

CHAR\_XDATA DMAP1\_TAR\_1, 0ff10H

CHAR\_XDATA DMAP1\_TAR\_2, 0ff11H

CHAR\_XDATA DMAP1\_SRC, 0ff12H

CHAR\_XDATA DMAP1\_CTL, 0ff13H

CHAR\_XDATA DMAP2\_TAR\_0, 0ff14H

CHAR\_XDATA DMAP2\_TAR\_1, 0ff15H

CHAR\_XDATA DMAP2\_TAR\_2, 0ff16H

CHAR\_XDATA DMAP2\_SRC, 0ff17H

CHAR\_XDATA DMAP2\_CTL, 0ff18H

CHAR\_XDATA DMAP3\_TAR, 0ff19H

CHAR\_XDATA DMAP3\_SRC, 0ff1aH

CHAR\_XDATA DMAP3\_CTL, 0ff1bH

; -- reserved --

; -- reserved --

; -- reserved --

; -- reserved --

CHAR\_XDATA DMASADR0\_0, 0ff20H

CHAR\_XDATA DMASADR0\_1, 0ff21H

CHAR\_XDATA DMASADR0\_2, 0ff22H

CHAR\_XDATA DMASADR0\_3, 0ff23H

CHAR\_XDATA DMASCNT0\_0, 0ff24H

CHAR\_XDATA DMASCNT0\_1, 0ff25H

CHAR\_XDATA DMASCNT0\_2, 0ff26H

CHAR\_XDATA DMACTRL0\_0, 0ff27H

CHAR\_XDATA DMACTRL0\_1, 0ff28H

CHAR\_XDATA DMAEINT0, 0ff29H

CHAR\_XDATA DMAINT0, 0ff2aH

CHAR\_XDATA DMACADR0\_0, 0ff2bH

CHAR\_XDATA DMACADR0\_1, 0ff2cH

CHAR\_XDATA DMACADR0\_2, 0ff2dH

CHAR\_XDATA DMACADR0\_3, 0ff2eH

CHAR\_XDATA DMACCNT0\_0, 0ff2fH

CHAR\_XDATA DMACCNT0\_1, 0ff30H

CHAR\_XDATA DMACCNT0\_2, 0ff31H

CHAR\_XDATA DMAPREQ0\_0, 0ff32H

CHAR\_XDATA DMAPREQ0\_1, 0ff33H

CHAR\_XDATA DMASADR1\_0, 0ff34H

CHAR\_XDATA DMASADR1\_1, 0ff35H

CHAR\_XDATA DMASADR1\_2, 0ff36H

CHAR\_XDATA DMASADR1\_3, 0ff37H

CHAR\_XDATA DMASCNT1\_0, 0ff38H

CHAR\_XDATA DMASCNT1\_1, 0ff39H

CHAR\_XDATA DMASCNT1\_2, 0ff3aH

CHAR\_XDATA DMACTRL1\_0, 0ff3bH

CHAR\_XDATA DMACTRL1\_1, 0ff3cH

CHAR\_XDATA DMAEINT1, 0ff3dH

CHAR\_XDATA DMAINT1, 0ff3eH

CHAR\_XDATA DMACADR1\_0, 0ff3fH

CHAR\_XDATA DMACADR1\_1, 0ff40H

CHAR\_XDATA DMACADR1\_2, 0ff41H

CHAR\_XDATA DMACADR1\_3, 0ff42H

CHAR\_XDATA DMACCNT1\_0, 0ff43H

CHAR\_XDATA DMACCNT1\_1, 0ff44H

CHAR\_XDATA DMACCNT1\_2, 0ff45H

CHAR\_XDATA DMAPREQ1\_0, 0ff46H

CHAR\_XDATA DMAPREQ1\_1, 0ff47H

CHAR\_XDATA DMACRC\_0, 0ff48H

CHAR\_XDATA DMACRC\_1, 0ff49H

CHAR\_XDATA PROTECT, 0ff60H

CHAR\_XDATA SECURITY, 0ff61H

CHAR\_XDATA PWDSEL, 0ff62H

CHAR\_XDATA PORCTRL, 0ff63H

CHAR\_XDATA DMAP4\_TAR\_0, 0ff80H

CHAR\_XDATA DMAP4\_TAR\_1, 0ff81H

CHAR\_XDATA DMAP4\_TAR\_2, 0ff82H

CHAR\_XDATA DMAP4\_SRC, 0ff83H

CHAR\_XDATA DMAP4\_CTL, 0ff84H

CHAR\_XDATA DMAP5\_TAR\_0, 0ff85H

CHAR\_XDATA DMAP5\_TAR\_1, 0ff86H

CHAR\_XDATA DMAP5\_TAR\_2, 0ff87H

CHAR\_XDATA DMAP5\_SRC, 0ff88H

CHAR\_XDATA DMAP5\_CTL, 0ff89H